CLAIM AMENDMENTS

1. (original) A PLL (Phase Locked Loop) implemented to perform high precision continuous time BPF (Band Pass Filter) tuning, the PLL comprising:

a PFD (Phase/Frequency Detector) that is operably coupled to determine a phase difference between transitions of a feedback signal and an input signal;

a CP (Charge Pump) operably coupled to convert the phase difference into a charge pump current;

a loop filter operably coupled to convert the charge pump current into a VCO (Voltage Controlled Oscillator) control voltage;

a VCO (Voltage Controlled Oscillator) operably coupled to convert the VCO control voltage into a recovered clock, wherein the feedback signal is derived from the recovered clock;

wherein the VCO includes a plurality of g_m (transconductance) cells;

an amplitude detector that detects an amplitude of the recovered clock and that biases the plurality of g_m cells of the VCO such that the each g_m cell of the plurality of g_m cells operates substantially within its linear operating region;

wherein the loop filter is implemented as a LPF (Low Pass Filter) having a resistor and a capacitor connected in series such that the capacitor is shunted to ground;

wherein a BPF (Band Pass Filter) control voltage is selected from a node that connects the resistor and the capacitor; and

wherein the BPF control voltage determines a tuning frequency of a BPF to which the PLL is communicatively coupled.

2. (original) The PLL of claim 1, wherein:

the BPF is implemented as a g_mC (transconductance-capacitance) filter that includes at least one additional plurality of g_m cells; and

the plurality of g_m cells of the VCO and the at least one additional plurality of g_m cells of the g_mC filter both include substantially identical g_m cells.

3. (original) The PLL of claim 2, wherein:

the tuning frequency of the BPF is substantially a center frequency of the BPF; and

the BPF control voltage biases the at least one additional plurality of g_m cells of the VCO such that the each g_m cell of the at least one additional plurality of g_m cells operates substantially within its linear operating region.

4. (original) The PLL of claim 2, wherein:

the substantially identical g_m cells of the plurality of the plurality of g_m cells and the at least one additional plurality of g_m cells provide substantial immunity to environmental perturbation of the PLL and the BPF.

5. (original) The PLL of claim 4, wherein:

the environmental perturbation of the PLL and the BPF is at least one of a temperature change, a humidity change, and a change in a power supply voltage.

6. (original) The PLL of claim 1, wherein:

the input signal to the PFD has a frequency that is substantially a center frequency of the BPF.

7. (original) The PLL of claim 1, wherein:

the loop filter of the PLL substantially eliminates any spur or glitch content within the BPF control voltage.

8. (original) The PLL of claim 1, wherein:

the BPF control voltage is a continuous time analog voltage signal.

9. (original) The PLL of claim 1, wherein:

the PLL is implemented within an AFE (Analog Front End) of a communication device; and

the communication device is a transceiver or a receiver.

10. (original) A PLL (Phase Locked Loop) implemented to perform high precision continuous time BPF (Band Pass Filter) tuning, the PLL comprising:

a PFD (Phase/Frequency Detector) that is operably coupled to determine a phase difference between transitions of a feedback signal and an input signal;

a CP (Charge Pump) operably coupled to convert the phase difference into a charge pump current;

a loop filter operably coupled to convert the charge pump current into a VCO (Voltage Controlled Oscillator) control voltage;

a VCO (Voltage Controlled Oscillator) operably coupled to convert the VCO control voltage into a recovered clock, wherein the feedback signal is derived from the recovered clock;

wherein the VCO includes a plurality of g_m (transconductance) cells;

an amplitude detector that detects an amplitude of the recovered clock and that biases the plurality of g_m cells of the VCO such that the each g_m cell of the plurality of g_m cells operates substantially within its linear operating region;

wherein the loop filter is implemented as a LPF (Low Pass Filter) having a resistor and a capacitor connected in series such that the capacitor is shunted to ground;

wherein a BPF (Band Pass Filter) control voltage is selected from a node that connects the resistor and the capacitor;

wherein the BPF control voltage determines a tuning frequency of a BPF to which the PLL is communicatively coupled;

wherein the BPF is implemented as a g_mC (transconductance-capacitance) filter that includes at least one additional plurality of g_m cells;

wherein the plurality of g_m cells of the VCO and the at least one additional plurality of g_m cells of the g_mC filter both include substantially identical g_m cells;

wherein the input signal to the PFD has a frequency that is substantially a center frequency of the BPF;

wherein the tuning frequency of the BPF is substantially a center frequency of the BPF; and

wherein the BPF control voltage biases the at least one additional plurality of g_m cells of the VCO such that the each g_m cell of the at least one additional plurality of g_m cells operates substantially within its linear operating region.

11. (original) The PLL of claim 10, wherein:

the substantially identical g_m cells of the plurality of the plurality of g_m cells and the at least one additional plurality of g_m cells provide substantial immunity to environmental perturbation of the PLL and the BPF.

12. (original) The PLL of claim 10, wherein:

the BPF control voltage is a continuous time analog voltage signal.

13. (original) The PLL of claim 10, wherein:

the loop filter of the PLL substantially eliminates any spur or glitch content within the BPF control voltage.

14. (original) The PLL of claim 10, wherein:

the PLL is implemented within an AFE (Analog Front End) of a communication device; and

the communication device is a transceiver or a receiver.

15. (original) A method for performing continuous time tuning to a BPF (Band Pass Filter), the method comprising:

oscillating a VCO (Voltage Controlled Oscillator) of a PLL (Phase Locked Loop) at a center frequency of a BPF (Band Pass Filter), wherein the PLL is communicatively coupled to the BPF;

adjusting an amplitude of an output of the VCO to ensure that each g_m (transconductance) cell of a plurality of g_m cells of the VCO operates within its respective linear region;

selecting an BPF control voltage from a loop filter of the PLL; and

providing the selected BPF control voltage from the loop filter of the PLL to the BPF thereby tuning the BPF to operate at its center frequency.

16. (original) The method of claim 15, wherein:

the BPF is implemented as a g_mC (transconductance-capacitance) filter that includes at least one additional plurality of g_m cells; and

the plurality of g_m cells of the VCO and the at least one additional plurality of g_m cells of the g_mC filter both include substantially identical g_m cells.

17. (original) The method of claim 16, wherein:

the substantially identical g_m cells of the plurality of the plurality of g_m cells and the at least one additional plurality of g_m cells provide substantial immunity to environmental perturbation of the PLL and the BPF

18. (original) The method of claim 16, further comprising:

operating each g_m cell of the at least one additional plurality of g_m cells of the BPF substantially within its linear operating region.

19. (original) The method of claim 15, wherein:

the loop filter of the PLL is implemented as a LPF (Low Pass Filter) having a resistor and a capacitor connected in series such that the capacitor is shunted to ground; and

further comprising:

selecting the BPF control voltage from a node that connects the resistor and the capacitor.

20. (original) The method of claim 15, wherein:

the method is performed within a communication device; and

the communication device is a transceiver or a receiver.